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PATENT ABSTRACTS OF JAPAN

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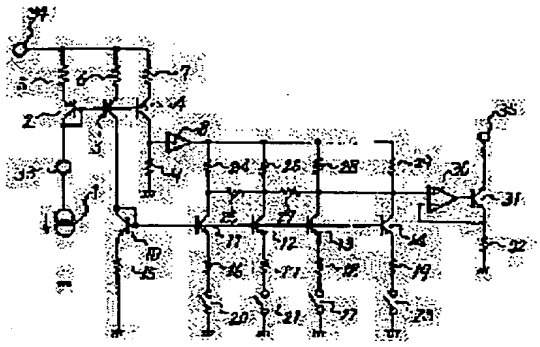
(54) CURRENT OUTPUT TYPE D/A CONVERTER CIRCUIT

(57)Abstract:
PURPOSE: To set the variable range of the output current optional by connecting a reference current source to a 1st current mirror circuit, using an output of a 1st amplifier for a reference potential application point and giving 1st to n-th outputs of a 2nd current mirror circuit to n-sets of weighting terminals of an R-2R resistor ladder circuit.
CONSTITUTION: A current of a reference current source 1 is given to a 1st current mirror circuit comprising transistors(TRs) 2-3 and resistors 5-7, its 1st output is inputted to a current-voltage circuit comprising a resistor 9 and an amplifier 8, in which the output is converted into a voltage and it is used for a reference voltage for an R-2R ladder circuit comprising resistors 24-29. A 2nd output of the 1st current mirror circuit is given to a 2nd current mirror circuit having n-sets of outputs comprising TRs 10-14 and resistors 15-19 and n-sets of outputs are given to n-sets of control current terminals to the R-2R resistor ladder circuit via switches 20-23 to decide an output voltage of the R-2R resistor ladder circuit.



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CLAIMS

[Claim(s)]
[Claim 1] The source of reference current is connected to the input of the 1st current Miller circuit with two outputs. The 1st output of said 1st current Miller circuit is connected to the end of the 1st resistance and the input of the 1st amplifier in which the other end was grounded. The equipotential terminal of the point supplying [reference potential], nothing, and an R-2R resistance ladder is connected to the above and the point supplying [reference potential] for the output of this 1st amplifier. The 2nd output of said 1st current Miller circuit Connect with the input of the 2nd current Miller circuit with the output of n pieces, and this input consists of the 2nd transistor with which the emitter was grounded through the 2nd resistance. The 3rd transistor which constitutes the 1st output of said 2nd current Miller circuit is grounded through the 1st switch controlled by the 1st bit of the 3rd resistance and a digital input signal. The 4th transistor which constitutes the 2nd output is grounded through the 2nd switch controlled by the 2nd bit of the 4th resistance and said digital input signal. The 5th transistor which constitutes the n-th output similarly is grounded through the n-th switch controlled by the n-th bit of the 5th resistance and said digital input signal. The n-th output is inputted into n weighting terminals of said R-2R resistance ladder from the 1st output of said 2nd current Miller circuit. The output of said R-2R resistance ladder The base of the 6th transistor is connected to an output and an emitter connects with the noninverting input of the 2nd amplifier with which the other end was grounded and which was connected to the reversal input with one edge of the 6th resistance. The current-output mold digital to analog circuit characterized by making the collector of said 6th transistor with a current outgoing end.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to a current-output mold digital to analog circuit about a digital to analog circuit.
[0002] There is a circuit which generally controls the output current by the digital input signal based on the reference current inputted as a current-output mold digital to analog circuit.
[0003] An example of the conventional current-output mold digital to analog circuit is shown in drawing 2 .
[0004] In drawing, it constitutes from a transistor 36 of the same configuration, a transistor 37, and resistance 38 and resistance 39 of the same resistance, the input of said current Miller circuit is connected to the source 1 of reference current in the 1st current Miller circuit which connected one terminal of resistance 38 and resistance 39 to the power supply terminal, and an output is connected to the input of the 2nd current Miller circuit.
[0005] The 2nd current Miller circuit carries out through touch-down of the transistor 40 and resistance 45 used as the input of current Miller circuit. The 1st output outputs the same current as the same transistor 41 and the resistance 45 as a transistor 40, the resistance 46 of the same resistance, and the source of reference current constituted from a circuit grounded with the switch 20 controlled by the 1st bit of a digital input signal. The 2nd output is constituted from a circuit grounded with the switch 21 controlled by the transistor 42 twice the area of a transistor 40, one half of the resistance 47 of a value of resistance 45, and the 2nd bit of a digital input signal. Output a twice as many current as the source of reference current, and constitute the 3rd output from a circuit grounded with the switch 22 controlled by the transistor 43 with a transistor 4 times the area of 40, one fourth of the resistance 48 of resistance of resistance 45, and the 3rd bit of a digital input signal, and it outputs a 4 times as many current as the source of reference current. The n-th output is 2n-1 of a transistor 40 similarly. A twice as many area as this 2n-1 of the transistor 44 which it has, and resistance 45 a part -- the circuit grounded with the switch 23 controlled by the resistance 49 of the resistance of 1, and the n-th bit of a digital input signal -- constituting -- 2n-1 of the source of reference current It constitutes from a circuit which outputs a twice as many current as this. It has the output terminal which connects from the 1st output of the 2nd current Miller circuit to the n-th output to all.
[0006] Next, actuation of the conventional example is explained.
[0007] The digital input signal constituted from n bits is inputted into each switch. If only the signal of the 1st bit is set to H, a switch 20 will turn on and the same current as the source of reference current will flow to an output terminal. If only the signal of the 2nd bit is set to H, a switch 21 turns on, a twice as many current as the source of reference current flows to an output terminal and the 1st bit and 2nd bit turn on in coincidence, a 3 times as many current as the source of reference current will flow to an output terminal. If all the n bits turn on similarly, - 1 time as many 2n current as this will be the digital to analog circuit which flows to an output terminal.
[0008] Therefore, it is IOUT about the current which flows to an output terminal. If it carries out and the current value of the source of reference current is set to Iref, it can express with a degree type.
[0009] IOUT =Iref (Z1+2Z2+4Z3+ -- +2n-1 Zn)
Zn The n-th bit substitutes 0 at the time of 1 and OFF at the time of ON.
[0010]
[Problem(s) to be Solved by the Invention] In this conventional current-output mold digital to analog circuit, the current value which only control of the current value of an integral multiple can be performed based on the current value of the source of reference current, and cannot choose the adjustable range as arbitration, and carries out adjustable has the problem limited by the current value of the source of reference current.
[0011] Moreover, if the surface ratio of the transistor which constitutes current Miller circuit becomes important in order to obtain the linearity of the output current and the bit of a digital input signal increases, in order for the transistor which constitutes current Miller circuit to increase exponentially and to carry out adjustable [of the very small range], the current value of the source of reference current needs to lessen, and there is a problem said that the resistance which constitutes current Miller circuit becomes large.
[0012] Next, if an actual value is put in and it explains to a detail, the current input-current-output mold digital to analog circuit which carries out adjustable [of the output current value] between 15microA and 30microA by the digital input signal of four bits will be considered.
[0013] Although change of 1microper step A will be needed and the digital input signal of four bits will make this the current value of the source of reference current if the current value which carries out adjustable is broken by the adjustable step since it serves as a setup of 16 steps Since adjustable [from 0microA to 15microA] is made in case of as it is, it is necessary to connect the current source of 15microA to an output terminal in addition to the source of reference current, and adjustable [from 15microA to 30microA] becomes possible by using this 2nd current source.
[0014] Next, when considering the resistance which constitutes current Miller circuit using it inside IC, when the current value of the source of reference current sets to 1microA,-two resistance of 300Kohm is needed [considering a transistor and the variation of resistance, it is necessary to set the electrical potential difference generated to the both ends of resistance as about 0.3V, and] in the 1st current Miller circuit.
[0015] Moreover, many resistance of high resistance [resistance / whose resistance of 300Kohm is 2 and 150Kohm], such as one, is needed, and use by IC has unreasonableness even in the 2nd current Miller circuit.

[0016]
[Means for Solving the Problem] The current-output mold digital to analog circuit of this invention connects the source of reference current to the collector of the 1st transistor used as the input of the 1st current Miller circuit with two outputs. The emitter of three transistors which constitute said 1st current Miller circuit is connected to a power supply terminal through resistance. The 1st output is connected to the input of the current-electrical-potential-difference conversion circuit which consists of the 1st amplifier and the 1st resistance, and said 1st resistance generates the electrical potential difference which was grounded and carried out the multiplication of the resistance to reference current, and is inputted as an equipotential terminal of an R-2R resistance ladder through the 1st amplifier 1 time the amplification factor of this.
[0017] The 2nd output of said 1st current Miller circuit is connected to the collector of the 2nd transistor used as the input of the 2nd current Miller circuit with the output of n pieces. The emitter of said 2nd transistor which constitutes the input of said 2nd current Miller circuit is grounded through the 2nd resistance. The 3rd transistor which constitutes the 1st output is grounded with the 1st switch controlled by the 1st bit of the 3rd resistance and a digital input signal. The 4th transistor which constitutes the 2nd output is grounded with the 2nd switch controlled by the 2nd bit of the 4th resistance and said digital input signal. The 5th transistor which constitutes the n-th output similarly is grounded with the n-th switch controlled by the n-th bit of the 5th resistance and said digital input signal. From the 1st output of said 2nd current Miller circuit to the n-th output It is inputted into n weighting terminals of a ****** R-2R resistance ladder.
[0018] The output of said R-2R resistance ladder was connected to the noninverting input of the 2nd amplifier, said 2nd amplifier inputted the output into the base of the 6th transistor, the emitter of said 6th transistor was grounded through connecting with the reversal input of said 2nd amplifier, and the 6th resistance, the voltage-current conversion circuit was constituted, and the collector of said transistor is equipped with the voltage-current conversion circuit linked to an output terminal.
[0019]
[Example] Next, this invention is explained with reference to a drawing.
[0020] Drawing 1 is the circuit diagram showing one example of this invention.
[0021] It connects with the input of the 1st current Miller circuit with the output of two pieces which constitutes the current of the source 1 of reference current from transistors 2, 3, and 4 and resistance 5, 6, and 7, and it inputs into the current-potential circuit constituted from the 1st output of said 1st current Miller circuit with resistance 9 and amplifier 8, changes into an electrical potential difference, and considers as the reference voltage of the R-2R resistance ladder constituted from resistance 24 by resistance 29.
[0022] It is Iref about the current value of the source 1 of reference current. It carries out and is Vref about the electrical potential difference of the output of a current-potential circuit. It will be set to Vref =R9xIref if it carries out.
[0023] Next, the 2nd output of said 1st current Miller circuit is connected to the input of the 2nd current Miller circuit which has the output of n pieces constituted from resistance 19 from a transistor 14 and resistance 15 from a transistor 10, and the output of n pieces is inputted into n control current terminals to said R-2R resistance ladder with a switch 23 from the switch 20 controlled by the digital input signal, and determines the output voltage of an R-2R resistance ladder.
[0024] When the criteria resistance of an R-2R resistance ladder is set to R, output voltage VR-2R of an R-2R resistance ladder is VR-2 R=Vref-RxIref x (Zn+ -- +Z2/2n-1+Z1 / 2n).
Zn The n-th bit substitutes 0 at the time of 1 and OFF at the time of ON. It becomes.
[0025] The output of an R-2R resistance ladder is connected with an amplifier 30 and a transistor 31 at the input of the voltage-current circuit constituted from resistance 32, it connects with an output terminal and the collector of a transistor 31 constitutes a current-output mold digital to analog circuit.
[0026] The output current Iout of this circuit It can be found by the following formula.
[0027] IOUT =VR-2 R/R32=(R9/R32) Iref-(R/R32) Iref (Zn+ -- +Z2/2n-1+Z1 / 2n)
The current-output mold digital to analog circuit which carries out adjustable [of the output current value] between 15microA and 30microA is considered by the digital input signal of four bits explained in the conventional example.
[0028] The maximum current value A of 30micro of the output current can be first found by the following formula.
[0029] Iout =(R9/R32) Iref -- it will be set to R9=60Kohm and R32=120Kohm, if the current value of the source of reference current is set to 60microA here and output voltage of a current-electrical-potential-difference conversion circuit is set to 3.6V.
[0030] Next, the minimum current value A of 15micro of the output current can be found by the following formula.
[0031] Iout =(R9/R32)Iref -(R/R32)Iref (8/15)
It is set to R=16Kohm. Moreover, the resistance which constitutes current Miller circuit serves as 5Kohm, and is a value which is satisfactory also as for use by IC.
[0032]
[Effect of the Invention] Since this invention enabled it to decide the current value of an output terminal to have explained above regardless of the current value of the source of reference current, even if it can set the adjustable range of the output current as arbitration and the number of bits of a digital input signal increases, also to adjustable [of the very small range], the number of a transistor and the value of resistance can be made small and it has the result that it is effective to contraction of a chip in IC-izing.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The circuit diagram of the example of this invention
[Drawing 2] The circuit diagram of the conventional example
[Description of Notations]
1 Source of Reference Current
2-4, 10-14, 31, 36-37, 40-44 Transistor
5-7, 9, 15-19, 24-29, 32, 38, 39, 45-49 Resistance
8 30 Amplifier
20-23 Switch
33 Input Terminal
34 Power Supply Terminal
35 Output Terminal

[Translation done.]

[0002]

Typically, a current output-type digital/analog conversion circuit receives a reference current to control an output current with the use of a digital input signal.

[0003]

Fig. 2 shows one example of such a conventional current output-type digital/analog conversion circuit.

[0004]

As shown in Fig. 2, transistors 36 and 37 are identical in shape to each other, and resistors 38 and 39 are identical in resistance value to each other. Each of the resistors 38 and 39 has one terminal corresponding to a first current mirror circuit connected to a power supply terminal. The current mirror circuit has an input connected to a reference current source 1 and an output connected to an input of a second current mirror circuit.

[0005]

The second current mirror circuit is grounded through a transistor 40 and a resistor 45 each serving as an input of the current mirror circuit. The second current mirror has first to "n"th outputs. Herein, the first output is configured by a circuit grounded through a transistor 41 which is identical in shape to the transistor 40, a resistor 46 which is identical in resistance value to the resistor

45, and a switch 20 which is controlled by a first bit of the digital input signal, and outputs a current which is equal to the current from the reference current source. The second output is configured by a circuit grounded through a transistor 42 which is twice larger in area than the transistor 40, a resistor 47 which is smaller in resistance value than the resistor 45 by one-half, and a switch 21 which is controlled by a second bit of the digital input signal, and outputs a current which is twice larger than the current from the reference current source. The third output is configured by a circuit grounded through a transistor 43 which is four times larger in area than the transistor 40, a resistor 48 which is smaller in resistance value than the resistor 45 by one-quarter, and a switch 22 which is controlled by a third bit of the digital input signal, and outputs a current which is four times larger than the current from the reference current source. Likewise, the "n"th output is configured by a circuit grounded through a transistor 44 which is 2^{n-1} times larger in area than the transistor 40, a resistor 49 which is smaller in resistance value than the resistor 45 by $1/2^{n-1}$, and a switch 23 which is controlled by an "n"th bit of the digital input signal, and outputs a current which is 2^{n-1} times larger than the current from the reference current source. Herein, the first to "n"th outputs of the second current mirror

circuit are connected to an output terminal.

[0006]

Next, description will be given of operations of the conventional current output-type digital/analog conversion circuit.

[0007]

The digital input signal composed of the "n" bits are supplied to the switches, respectively. When only the signal corresponding to the first bit becomes HIGH, the switch 20 is turned ON. Thus, a current which is equal to the current from the reference current source is fed to the output terminal. When only the signal corresponding to the second bit becomes HIGH, the switch 21 is turned ON. Thus, a current which is twice larger than the current from the reference current source is fed to the output terminal. When the first bit and the second bit are turned ON simultaneously, a current which is three times larger than the current from the reference current source is fed to the output terminal. Likewise, when all the "n" bits are turned ON, a current which is 2^{n-1} times larger than the current from the reference current source is fed to the output terminal.

[0008]

Accordingly, the following equation is established.

[0009]

$$I_{out} = I_{ref} \ (Z_1 + 2Z_2 + 4Z_3 + \ldots + 2^{n-1}Z_n)$$

In this equation, I_{out} represents a current fed to the output terminal, and I_{ref} represents a current value of the reference current source. Moreover, 1 is substituted for Zn when the "n"th bit is turned ON, and 0 is substituted for Zn when the "n"th bit is turned OFF.

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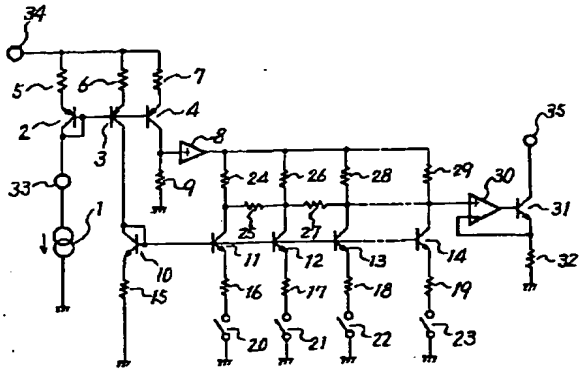
(54)【発明の名称】　電流出力型デジタル／アナログ変換回路

(57)【要約】
【目的】基準電流源から入力する電流値に関係なく出力端子から出力する電流の可変範囲を任意に設定でき、微少な範囲の可変にも対応できる。
【構成】基準電流源の電流をカレントミラー回路を介して、電流－電圧変換回路に入力し基準電位供給点を作り、ｎ個のビットで構成するデジタル入力信号により基準電流源をもとに作られた電流をＲ－２Ｒ抵抗ラダー回路のｎ個の重み付け端子に入力し、出力電圧を制御する。この出力電圧は、電圧－電流変換回路により電流として出力端子より出力する電流出力型デジタル／アナログ変換回路。



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【特許請求の範囲】

【請求項1】　基準電流源を、2つの出力を持つ第1のカレントミラー回路の入力に接続し、前記第1のカレントミラー回路の第1の出力は他端が接地された第1の抵抗の一端と第1の増幅器の入力に接続し、該第1の増幅器の出力を基準電位供給点となし、R－2R抵抗ラダー回路の等電位端子を前記、基準電位供給点に接続し、前記第1のカレントミラー回路の第2の出力は、n個の出力を持つ第2のカレントミラー回路の入力に接続し、該入力はエミッタが第2の抵抗を介して接地された第2のトランジスタで構成され、前記第2のカレントミラー回路の第1の出力を構成する第3のトランジスタは第3の抵抗とデジタル入力信号の第1のビットで制御する第1のスイッチを介して接地し、第2の出力を構成する第4のトランジスタは第4の抵抗と前記デジタル入力信号の第2のビットで制御する第2のスイッチを介して接地し、同様に第nの出力を構成する第5のトランジスタは第5の抵抗と前記デジタル入力信号の第nのビットで制御する第nのスイッチを介して接地され、前記第2のカレントミラー回路の第1の出力から第nの出力までは前記R－2R抵抗ラダー回路のn個の重み付け端子に入力され、前記R－2R抵抗ラダー回路の出力は、第6のトランジスタのベースが出力に接続され、エミッタが他端が接地された第6の抵抗の1端とともに反転入力に接続された第2の増幅器の非反転入力に接続し、前記第6のトランジスタのコレクタを電流出力端となすことを特徴とした電流出力型デジタル／アナログ変換回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はデジタル／アナログ変換回路に関し、特に電流出力型デジタル／アナログ変換回路に関する。

【0002】一般に、電流出力型デジタル／アナログ変換回路として入力された基準電流をもとにし、デジタル入力信号で出力電流を制御する回路がある。

【0003】従来の電流出力型デジタル／アナログ変換回路の一例を図2に示す。

【0004】図において同一形状のトランジスタ36とトランジスタ37，同一抵抗値の抵抗38と抵抗39で構成し、抵抗38と抵抗39の一方の端子は電源端子に接続した第1のカレントミラー回路で、前記カレントミラー回路の入力は基準電流源1に接続し、出力は第2のカレントミラー回路の入力に接続する。

【0005】第2のカレントミラー回路は、カレントミラー回路の入力となるトランジスタ40と抵抗45を通し接地し、第1の出力はトランジスタ40と同一のトランジスタ41と抵抗45と同一抵抗値の抵抗46とデジタル入力信号の第1のビットで制御するスイッチ20で接地した回路で構成する基準電流源と同じ電流を出力し、第2の出力はトランジスタ40の2倍の面積のトランジスタ42と抵抗45の1／2の値の抵抗47とデジタル入力信号の第2のビットで制御するスイッチ21で接地した回路で構成し、基準電流源の2倍の電流を出力し、第3の出力はトランジスタ40の4倍の面積を持つトランジスタ43と抵抗45の1／4の抵抗値の抵抗48とデジタル入力信号の第3のビットで制御するスイッチ22で接地した回路で構成し基準電流源の4倍の電流を出力し、同様に第nの出力はトランジスタ40の2^{n-1}倍の面積を持つトランジスタ44と抵抗45の2^{n-1}分の1の抵抗値の抵抗49とデジタル入力信号の第nのビットで制御するスイッチ23で接地した回路で構成し基準電流源の2^{n-1}倍の電流を出力する回路で構成し、第2のカレントミラー回路の第1の出力から第nの出力までを全てに接続する出力端子を有している。

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【0006】次に、従来例の動作について説明する。

【0007】n個のビットで構成するデジタル入力信号を各々のスイッチに入力し、第1のビットの信号のみがHになるとスイッチ20がONして出力端子に基準電流源と同じ電流が流れ、第2のビットの信号のみがHになるとスイッチ21がONして出力端子に基準電流源の2倍の電流が流れ、第1のビットと第2のビットが同時にONすれば出力端子に基準電流源の3倍の電流が流れる。同様にn個のビットの全てがONすれば2^n-1倍の電流が出力端子に流れるデジタル／アナログ変換回路である。

【0008】したがって出力端子に流れる電流をI_{out}とし、基準電流源の電流値をIrefとすると次式で表わすことができる。

【0009】$I_{out}=I_{ref}(Z_1+2Z_2+4Z_3+\cdots+2^{n-1}Z_n)$

Z_nは第nのビットがON時1、OFF時0を代入する。

【0010】

【発明が解決しようとする課題】この従来の電流出力型デジタル／アナログ変換回路では、基準電流源の電流値を元に整数倍の電流値の制御しかできず、可変範囲を任意に選べず、また可変する電流値は基準電流源の電流値により限定される問題がある。

【0011】又、出力電流のリニアリティを得る為には、カレントミラー回路を構成するトランジスタの面積比が重要となり、デジタル入力信号のビットが多くなるとカレントミラー回路を構成するトランジスタが指数的に増加し、又微少な範囲を可変する為には、基準電流源の電流値が少なくする必要があり、カレントミラー回路を構成する抵抗値が大きくなると言う問題がある。

【0012】次に実際の値を入れて詳細に説明すると、4個のビットのデジタル入力信号により出力電流値を15μAから30μAの間で可変する電流入力－電流出力型デジタル／アナログ変換回路を考える。

【0013】4個のビットのデジタル入力信号は16ス

テップの設定となる為、可変する電流値を可変ステップで割ると1ステップ当り1μAの変化が必要となり、これを基準電流源の電流値とするが、このままだと0μAから15μAまでの可変しかできない為、基準電流源以外に15μAの電流源を出力端子に接続する必要があり、この2個目の電流源を使用することにより15μAから30μAまでの可変が可能となる。

【0014】次にカレントミラー回路を構成する抵抗値について考えると、ICの内部で使用する場合、トランジスタや抵抗のバラツキを考えると抵抗の両端に発生する電圧を0．3V程度に設定する必要があり、基準電流源の電流値が1μAとすると第1のカレントミラー回路では300KΩの抵抗が2本必要となる。

【0015】又、第2のカレントミラー回路でも300KΩの抵抗が2本、150KΩの抵抗が1本、など高抵抗値の抵抗が数多く必要となり、ICでの使用には無理がある。

【0016】

【課題を解決するための手段】本発明の電流出力型デジタル／アナログ変換回路は基準電流源を、2つの出力を持つ第1のカレントミラー回路の入力となる第1のトランジスタのコレクタに接続し、前記第1のカレントミラー回路を構成する3個のトランジスタのエミッタは抵抗を介して電源端子に接続され、第1の出力は第1の増幅器と第1の抵抗とで構成される電流－電圧変換回路の入力に接続され、前記第1の抵抗は接地され基準電流と抵抗値を乗算した電圧を発生し、増幅率1倍の第1の増幅器を通してR－2R抵抗ラダー回路の等電位端子として入力される。

【0017】前記第1のカレントミラー回路の第2の出力はn個の出力を持つ第2のカレントミラー回路の入力となる第2のトランジスタのコレクタに接続され、前記第2のカレントミラー回路の入力を構成する前記第2のトランジスタのエミッタは第2の抵抗を介して接地され、第1の出力を構成する第3のトランジスタは第3の抵抗とデジタル入力信号の第1のビットで制御する第1のスイッチで接地し、第2の出力を構成する第4のトランジスタは第4の抵抗と前記デジタル入力信号の第2のビットで制御する第2のスイッチで接地し、同様に第nの出力を構成する第5のトランジスタは第5の抵抗と前記デジタル入力信号の第nのビットで制御する第nのスイッチで接地され前記第2のカレントミラー回路の第1の出力から第nの出力までは前記R－2R抵抗ラダー回路のn個の重み付け端子に入力される。

【0018】前記R－2R抵抗ラダー回路の出力は第2の増幅器の非反転入力に接続し、前記第2の増幅器は、出力を第6のトランジスタのベースに入力し、前記第6のトランジスタのエミッタは、前記第2の増幅器の反転入力に接続するのと第6の抵抗を介して接地し、電圧－電流変換回路を構成し、前記トランジスタのコレクタは

出力端子に接続する電圧－電流変換回路を備えている。

【0019】

【実施例】次に、本発明について図面を参照して説明する。

【0020】図1は本発明の一実施例を示す回路図である。

【0021】基準電流源1の電流をトランジスタ2，3，4と抵抗5，6，7で構成する2個の出力を持つ第1のカレントミラー回路の入力に接続し、前記第1のカレントミラー回路の第1の出力より抵抗9と増幅器8で構成する電流－電圧回路に入力して電圧に変換し、抵抗24から抵抗29で構成するR－2R抵抗ラダー回路の基準電圧とする。

【0022】基準電流源1の電流値をI_{ref}とし、電流－電圧回路の出力の電圧をV_{ref}とすると

$V_{ref}=R9\times I_{ref}$

となる。

【0023】次に、前記第1のカレントミラー回路の第2の出力はトランジスタ10からトランジスタ14と抵抗15から抵抗19で構成するn個の出力を持つ第2のカレントミラー回路の入力に接続し、そのn個の出力はデジタル入力信号で制御されるスイッチ20からスイッチ23によって前記R－2R抵抗ラダー回路へのn個のコントロール電流端子に入力し、R－2R抵抗ラダー回路の出力電圧を決める。

【0024】R－2R抵抗ラダー回路の基準抵抗値をRとするとR－2R抵抗ラダー回路の出力電圧V_{R-2R}は

$V_{R-2R}=V_{ref}-R\times I_{ref}\times(Z_n+\cdots+Z_2/2^{n-1}+Z_1/2^n)$

Z_nは第nのビットがON時1、OFF時0を代入する。となる。

【0025】R－2R抵抗ラダー回路の出力は増幅器30，トランジスタ31と抵抗32で構成する電圧－電流回路の入力に接続され、トランジスタ31のコレクタは出力端子に接続し電流出力型デジタル／アナログ変換回路を構成する。

【0026】この回路の出力電流I_{out}は次の式で求まる。

【0027】$I_{out}=V_{R-2R}/R32$

$=(R9/R32)I_{ref}-(R/R32)I_{ref}(Z_n+\cdots+Z_2/2^{n-1}+Z_1/2^n)$

従来例で説明した、4個のビットのデジタル入力信号により、出力電流値を15μAから30μAの間で可変する電流出力型デジタル／アナログ変換回路を考える。

【0028】まず出力電流の最大電流値30μAは、次の式で求まる。

【0029】$I_{out}=(R9/R32)I_{ref}$

ここで基準電流源の電流値を60μAとし、電流－電圧変換回路の出力電圧を3．6Vとすると

R9＝60KΩ，R32＝120KΩ

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となる。

【0030】次に出力電流の最小電流値15μAは、次の式で求まる。

【0031】$I_{out} = (R9/R32) I_{ref} - (R/R32) I_{ref}$ (8／15)

R＝16KΩ

となる。又カレントミラー回路を構成する抵抗は、5KΩとなり、ICでの使用でも問題ない値である。

【0032】

【発明の効果】以上説明したように本発明は、基準電流源の電流値に関係なく、出力端子の電流値を決めることができる様にしたので、出力電流の可変範囲を任意に設定することができ、又、デジタル入力信号のビット数が増えても、微少な範囲の可変に対しても、トランジスタの個数や抵抗の値を小さくすることができ、IC化においてチップの縮小に対して効果があるという結果を有する。

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【図面の簡単な説明】

【図1】本発明の実施例の回路図

【図2】従来の例の回路図

【符号の説明】

1　基準電流源

2～4，10～14，31，36～37，40～44　トランジスタ

5～7，9，15～19，24～29，32，38，39，45～49　抵抗

8，30　増幅器

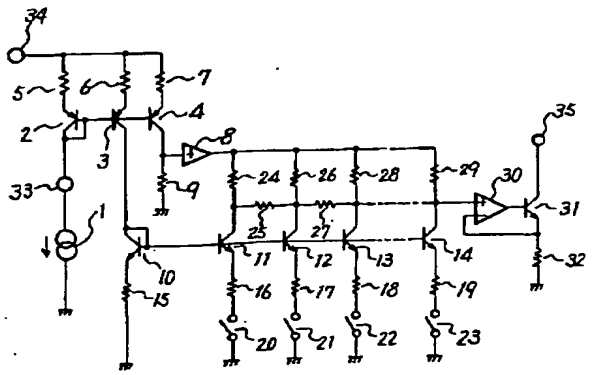
20～23　スイッチ

33　入力端子

34　電源端子

35　出力端子

【図1】



【図2】